

What is claimed is:

1. A semiconductor device comprising:
a semiconductor substrate of a first conductivity type having chip formation areas, the semiconductor substrate including:
scribe lanes formed therein to define chip formation areas;
a deep well area formed in each chip formation area, each deep well area having a second conductivity type opposite the first conductivity type; and
at least one well area formed within at least one deep well area.
2. The semiconductor device of claim 1, wherein,
the first conductivity type is a p-type conductor;
and
the second conductivity type is a n-type conductor.
3. The semiconductor device of claim 1, wherein,
the first conductivity type is a n-type conductor;
and
the second conductivity type is a p-type conductor.

4. The semiconductor device of claim 1, wherein a first well area of the first conductivity type and a second well area of the second conductivity type are separately formed within the deep well area.

5. A method for manufacturing a semiconductor device comprising:

preparing a semiconductor substrate of a first conductivity type;

forming scribe lanes in the semiconductor substrate, said scribe lanes defining chip formation areas;

forming a deep well area in each chip formation area, each deep well area having a second conductivity type opposite the first conductivity type; and

forming at least one well area within the deep well area.

6. The method of claim 6, further comprising forming a mask on the semiconductor substrate such that the deep well areas are formed in the chip formation areas and not in the scribe lanes.

7. The semiconductor device of claim 1, wherein, the first conductivity type is a p-type conductor;

and

the second conductivity type is a n-type conductor.

8. The semiconductor device of claim 6, wherein,
the first conductivity type is a p-type conductor;

and

the second conductivity type is a p-type conductor.

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~~10.~~ The method of claim 6, wherein a first
conductive well area and a second conductive well area
are separately formed within the deep well area.

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~~11.~~ The method of claim 10, wherein
the first conductive well area is formed of the
first conductivity type; and
the second conductive well area is formed of the
second conductivity type.

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~~12.~~ The method of claim 6, wherein the scribe lanes
are formed at all portions surrounding the chip
formation areas.

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~~13.~~ The method of claim 7, further comprising
removing the mask using plasma processing or plasma

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